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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,601	12/21/2000	James S. McCormick	1400.4100290	1003

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EXAMINER	
SCHEIBEL, ROBERT C	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,601	MCCORMICK ET AL.	
	Examiner	Art Unit	
	Robert C. Scheibel	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12,13,17 and 19-23* is/are rejected.

7)☒ Claim(s) *3-11,14-16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050915*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Amendment filed 6/27/2005 is acknowledged.
- Claim 1 has been amended.
- Claims 1-23 are pending.

Response to Arguments

1. Examiner acknowledges applicant's request for the previously cited references (on the form PTO-892 sent on 5/6/2004) to be included with the current action. The form PTO-892 included herein lists the references from the previous action as well.

2. Applicant's arguments, see paragraph 3 of page 8, filed 6/27/2005, with respect to the Dravida reference and claims 17, 19, and 21 have been fully considered but they are not persuasive. Applicant argues that the Dravida reference fails to establish inherency. Examiner respectfully disagrees with applicant on this point. Examiner asserts that inherency was properly argued in the remarks of the last office action. Since the routing change occurs in response to a change in congestion status, the routing change ***must*** be away from the routing. However, as the previous office action also provided further evidence of how Dravida teaches that the routing is made away from the congestion (applicant is referred to the last two sentences of paragraph 3 of the office action of 1/24/2005), the inherency argument is not necessary. As such, examiner has removed discussion of inherency from the present office action to avoid any further confusion on the record.

3. Applicant's arguments, see page 8, filed 6/27/2005, with respect to the rejection of claims 1-16 under 35 U.S.C. 112, second paragraph, have been fully considered and

are persuasive. The rejection of claims 1-16 under 35 U.S.C. 112, second paragraph, has been withdrawn.

4. Applicant's arguments, see page 9, filed 6/27/2005, with respect to the rejection of claims 1 and 2 under 35 U.S.C. 102(b) have been fully considered but they are not persuasive. Applicant argues that the statement indicating that the large buffer delay clearly indicates congestion is not supported by evidence in the reference. Applicant further questions the clarity of the phrase "large buffer delay". Regarding the first point, examiner refers applicant to the passage from lines 63-66 of column 1 of Barberis which very clearly that the first object of the invention is to eliminate congestion through the method of calculating incremental delays. As is clearly stated in the office action, this incremental delay discloses the congestion indication of the present invention; it is thus clear from the statement by Barberis (lines 63-66 of column 1) that the point of this incremental delay calculation is the elimination of congestion. Thus, the previous rejection is maintained. Regarding the second point, as indicated from the context of the phrase, it refers to a (relatively) large delay of a buffer.

5. Applicant's arguments, see page 9, filed 6/27/2005, with respect to the rejection of claim 12 under 35 U.S.C. 103(a) have been fully considered but are not persuasive. Applicant argues that the examiner does not provide any references or evidence to support the contention that it would have been obvious to implement the buffers of Barberis on separate line cards. Examiner respectfully disagrees with this argument. As indicated in the previous office action, the concept of a distributed architecture using multiple line cards is disclosed by the applicant's admitted prior art (AAPA). The advantages (increased capacity and easier upgradeability, for example) are well known in

the art. Furthermore, Barberis is merely silent as to the particular structure of the system (one card or multiple line cards) and the AAPA is relied upon to provide one of the possible implementations of Barberis.

6. Applicant's arguments, see page 9, filed 6/27/2005, with respect to the rejection of claims 17, 19, and 21 under 35 U.S.C. 103(a) have been fully considered but are not persuasive. Applicant argues that the examiner does not provide any references or evidence to support the contention that it would have been obvious to implement the buffers of Dravida on separate line cards. Examiner respectfully disagrees with this argument. As indicated in the previous office action, the concept of a distributed architecture using multiple line cards is disclosed by the applicant's admitted prior art (AAPA). The advantages (increased capacity and easier upgradeability, for example) are well known in the art. Furthermore, Dravida is merely silent as to the particular structure of the system (one card or multiple line cards) and the AAPA is relied upon to provide one of the possible implementations of Dravida.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1-2** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,320,500 to Barberis, et al.

Regarding claim **1**, Barberis discloses the limitation of a multiprocessor control block in Figure 1B. The plurality of distributed processors is included within the delay estimator ST of Figure 1B. The distributed processors are more clearly shown in Figure 2 which shows the n + 1 processing units (arithmetic units, summing registers, etc.) corresponding to each of the buffers of Figure 1B. The resource routing processor is the combination of the processor EL and the updating unit AG of Figure 1B which is clearly coupled to the distributed processors (delay estimator ST). More specifically, the delay estimator maintains congestion status of the queuing points (buffers) as the incremental delays assigned to the respective buffers; this is described throughout, for example in lines 8-14 of column 2. As is well known in the art, a large buffer delay indicates congestion and thus discloses the congestion indication of the claimed invention. Regarding the specific details of the resource routing processor, the processor EL controls the routing functionality within the communication switch as described throughout Barberis; see lines 1-8 of column 2, for example. Further, the processor and the updating unit preferentially select uncongested routes for subsequent connection within the switch based on the congestion indications as indicated in lines 49-52 of column 3 and lines 43-49 of column 4. The path with the minimal delay time is determined in part by the incremental delays of the buffers and thus is determined in part due to the congestion indications as stated above.

Regarding claim **2**, the resource routing processor performs resource allocation amongst the connections supported by the switch as discussed throughout, for example as indicated in lines 1-8 of column 2. This passage indicates that the processor controls the

transfer of incoming packets to the transmit buffers and thus allocates resources for the packets traversing the switch.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim **12** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,320,500 to Barberis et al in view of Applicant's admitted prior art.

Regarding claims **12**, Barberis discloses the limitations of parent claim 2 as discussed in the rejection under 35 U.S.C. 102 (b) above. Barberis discloses the limitation that the congestion indications (queue lengths) of the buffer memories in Figure 1B are used in the routing decision by the resource routing processor as described in the rejection above as well.

Barberis does not expressly disclose the limitation that the input and output buffers are implemented on separate line cards. Applicant's admitted prior art (Figure 1) clearly indicates the use of a plurality of line cards in a communications switch. Barberis and Applicant's admitted prior art are from the same field of endeavor of congestion control in a communications node. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Barberis to implement the input and output buffers of Figure 1B on separate line cards. The motivation for doing so would have been to allow the nodes of Barberis to have more capacity (N input/output cards can support more traffic than if all the buffers were implemented on a single card) and allow the system to be upgraded (to higher capacity) more easily. Therefore, it would have been obvious to combine Applicant's admitted prior art with Barberis for the purposes of greater capacity and easier upgradeability to obtain the invention as specified in claim 12.

6. Claims **17, 19, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,253,248 to Dravida et al in view of Applicant's admitted prior art.

Regarding claims **17 and 19**, Dravida discloses a communication switch in the node of Figure 27. The nodal processor 2730 discloses the routing control block (claim 17) and central control block (claim 19). The nodal processor performs routing functionality through the maintenance of the routing tables (2750 and 2760) and call processing through the update of the maintenance of topology information (2801 in Figure 28) and determining alternate paths for calls as the topology changes (lines 65-67 of column 11). The input buffers (2715-2717) and output buffers (2725-2727) of Figure 27 disclose the functionality of the plurality of line cards which are operably coupled

with the routing/central control block. As is shown in Figure 27 and the flow chart of Figure 26, then congestion is detected on a transmit queue (output buffer), a congestion indication (via the congestion monitor) is provided to the routing control block. The switch between the congestion monitor 2740 and the routing tables indicates how Dravida routes calls away from the congestion based on this indication.

Dravida does not expressly disclose the limitation that the input and output buffers are line cards. Applicant's admitted prior art (Figure 1) clearly indicates the use of a plurality of line cards in a communications switch. Dravida and Applicant's admitted prior art are from the same field of endeavor of congestion control in a communications node. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Dravida to implement the input and output buffers of Figure 27 on separate line cards. The motivation for doing so would have been to allow the nodes of Dravida to have more capacity (N input/output cards can support more traffic than if all the buffers were implemented on a single card) and allow the system to be upgraded (to higher capacity) more easily. Therefore, it would have been obvious to combine Applicant's admitted prior art with Dravida for the purposes of greater capacity and easier upgradeability to obtain the invention as specified in claims 17 and 19.

Regarding claim **21**, with the parent claim 19 addressed above, Dravida discloses the limitation of the subsequent routing operations including maintaining the status of a plurality of transmit queues (congestion monitor 2740) wherein the status is used to determine a non-congested compatible transmit queues for the subsequent routing operations (as indicated in lines 42-45 of column 5).

7. Claims **1-2, 12-13, 17, and 19-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,838,677 to Kozaki et al in view of U.S. Patent 5,802,040 to Park et al.

Regarding claim **1**, Kozaki discloses the limitation of a plurality of distributed processors (elements 30, 31, 36, 39, etc. of elements 3-x of Figure 9) that include ingress and egress queuing points corresponding to data units communicated within the communication switch (the buffers 35 and 38 of Figure 9), wherein when a congestion condition exists at selected queuing points within the one of the plurality of distributed processors, a congestion indication is generated (see lines 4-10 of column 14 and lines 7-9 of column 15). Kozaki does not disclose the limitation of the resource routing processor. Park discloses a resource routing processor (element 6 of Figure 1, see specifically element 13 of Figure 2) operably coupled to the plurality of distributed processors (operably coupled to the line cards as shown in both figures 1 and 2), wherein the resource routing processor controls routing functionality within the communication switch (see lines 10-16 of column 4), wherein the resource routing processor receives congestion indications (see lines 10-16 of column 4) and preferentially selects uncongested routes for subsequent connections within the communication switch based on the congestion indications (see lines 10-16 of column 4).

Regarding claim **17**, Kozaki discloses the limitation of a plurality of line cards (elements 3-1 to 3-n of Figure 9), wherein each of the line cards includes at least one transmit queue (element 38 of Figure 9), wherein when congestion is detected on a transmit queue, a congestion indication is provided (see lines 4-10 of column 14 and lines

7-9 of column 15). Kozaki does not disclose the limitation of the routing control block. Park discloses a routing control block that performs call processing operations within the switch (element 6 of Figure 1, see specifically element 13 of Figure 2). This routing control is operably coupled to the line cards as shown in both figures 1 and 2. The limitation that the routing control block routes calls away from congestion is disclosed in lines 10-16 of column 4.

Regarding claim **19**, Kozaki discloses the limitation of detecting congestion in a transmit queue corresponding to a line card and the limitation of providing an indication of the congestion to a central control block in lines 4-10 of column 14 and lines 7-9 of column 15. Kozaki does not disclose the limitation that the central control block performs call processing and routing for a plurality of line cards included in the communication switch, wherein the central control block performs subsequent routing operations in a manner that avoids the congestion corresponding to the line card. Park discloses the limitation that the central control block (element 6 of Figure 1, see specifically element 13 of Figure 2) performs call processing and routing for a plurality of line cards included in the communication switch, wherein the central control block performs subsequent routing operations in a manner that avoids the congestion corresponding to the line card (see lines 10-16 of column 4).

Kozaki and Park are analogous art because they are from the same field of endeavor of congestion control in communication systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Kozaki to use a centrally located processor to control routing in the switch (as taught by Park), based on the congestion information already transmitted to a central location in Park. The

motivation for doing so would have been to route the traffic that had been scheduled for a congested link to another link to recover from the congestion state as suggested by Park in lines 3-5 of column 4. Therefore, it would have been obvious to combine Park with Kozaki for the benefit of recovering from congestion to obtain the invention as specified in claims 1, 17, and 19.

Regarding claim **2**, the combination of Kozaki and Park used in the rejection of parent claim 1 also discloses the limitation that the resource routing processor performs resource allocation amongst connections supported by the switch (see lines 10-16 of column 4 of Park).

Regarding claim **12**, the combination of Kozaki and Park used in the rejection of parent claim 1 also discloses the limitation of a plurality of line cards (see elements 3-1 to 3-n of Figure 9 of Kozaki) operably coupled to the multiprocessor control block (as in the combination above), wherein the plurality of line cards include ingress and egress queuing points for line card data units (elements 35 and 38 of Figure 9 of Kozaki), wherein when a congestion condition exists at a queuing point within a line card, a line card congestion indication is generated (see lines 4-10 of column 14 and lines 7-9 of column 15 of Kozaki) and provided to the resource routing processor such that the resource routing processor selects routes at least partially based on line card congestion indications received (see lines 10-16 of column 4 of Park).

Regarding claim **13**, the combination of Kozaki and Park used in the rejection of parent claim 12 also discloses the limitation of a message processor operably coupled to the multiprocessor control block and the plurality of line cards, wherein the message processor supports messaging between the plurality of intermediate processors and the

plurality of line cards in element 39 of Figure 9 which supports the communication of the congestion information to the central control block.

Regarding claim **20**, the combination of Kozaki and Park used in the rejection of parent claim 19 discloses the limitation that the central control block includes a resource routing processor (element 13 of Figure 2 of Park), a plurality of intermediate processors (elements 12, 21-23, and 31-33 of Figure 2 of Park), and a link layer processor (element 20 and 30 of Figure 2 of Park), wherein the resource routing processor performs the subsequent routing operations (see lines see lines 10-16 of column 4 of Park).

Regarding claim **21**, the combination of Kozaki and Park used in the rejection of parent claim 19 discloses the limitation that performing subsequent routing operations includes maintaining status of a plurality of transmit queues corresponding to a plurality of line cards in the switch, wherein the status is used to determine a non-congested compatible transmit queues for the subsequent routing operations in lines 10-16 of column 4. The routing table represents the routing table represents the status and the link being affordable suggests that it doesn't contain a congestion status.

Regarding claim **22**, Kozaki discloses the limitation of prioritizing data flow in the switch such that congestion is concentrated at the plurality of transmit queues in lines 26-33 of column 10.

Regarding claim **23**, Kozaki discloses the limitation that the congestion in the transmit queue is a result of a buildup of messages corresponding to programming commands that are directed towards the line card. The congestion is due to a buildup of data in the buffer 38 of Figure 9 which are the result of programming commands that caused the packets to be transmitted through the switch to this buffer.

Allowable Subject Matter

8. Claims **3-11, 14-16, and 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5,926,456, 5,912,877, 5,854,899 all disclose congestion control methods related to the present application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Monday and Thursday from 6:30-5:00 Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RCS 9-15-05

Robert C. Scheibel
Examiner
Art Unit 2666

Seema S. Rao 9/19/05

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